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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/576,316	04/18/2006	Jeffrey A. Chapman	GB 030192	4470

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EXAMINER	
SMOOT, STEPHEN W	

ART UNIT	PAPER NUMBER
2813	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/576,316	CHAPMAN, JEFFREY A.	
	Examiner	Art Unit	
	Stephen W. Smoot	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 April 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office action is in response to application papers filed on 18 April 2006.

Specification

1. The disclosure is objected to because of the following informality: The specification lacks section headings as required per 37 CFR 1.77(c).

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-2, 4, 11-12 are rejected under 35 U.S.C. 102(b) as being anticipated by De Bruin et al. (US 5,063,169).

Referring to Figs. 1-2 and column 3, line 4 to column 5, line 44, De Bruin et al. disclose a method of forming conductive pillars (15) over a substrate (1) that includes using photolithographic and developing techniques to define openings (14) in a layer of photosensitive resist (13) and filling the openings (14) with nickel to form the pillars (15) by plating in a nickel-containing solution.

These are all of the process limitations as set forth in claims 1-2, 4 of the applicant's invention as well as all of the structural limitations as set forth in claims 11-12 of the applicant's invention.

4. Claims 1-6, 8, 11-12, 14, 16-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Capote et al. (US 5,716,663).

Referring to Fig. 7 and column 11, line 58 to column 12, line 33, Capote et al. disclose a method for producing multilayer circuits that includes applying a photoimageable dielectric layer to a substrate, patterning the photoimageable dielectric layer through exposure to light followed by developing to form grooves in the dielectric, filling the grooves with metal-containing conductive ink by doctor blading, and curing the conductive ink.

These are all of the process limitations as set forth in claims 1-6, 14, 16-17 of the applicant's invention as well as all of the structural limitations as set forth in claims 11-12 of the applicant's invention.

Regarding claim 8, this process can be repeated to form a multilayered structure as indicated in column 12, lines 22-33.

5. Claims 1-2, 4-6, 8, 11-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Ryu (US 5,747,222).

Referring to Figs. 1-2 and column 2, line 43 to column 3, line 65, Ryu discloses a method of forming a multilayered circuit substrate that includes coating a substrate (10) with a photosensitive insulating layer (20), patterning the insulating layer (20) through selective light exposure and developing to form spaces (22), filling the spaces (22) with conductive ink, and heating the conductive ink to form a conductive layer (30). The conductive ink includes metal powders as indicated in column 4, lines 10-15.

These are all of the process limitations as set forth in claims 1-2, 4-6 of the applicant's invention as well as all of the structural limitations as set forth in claims 11-12 of the applicant's invention.

Regarding claim 8, this process can be repeated to form a multilayered structure as indicated in column 3, lines 5-25.

6. Claims 1-6, 11-12, 14, 16-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Kydd et al. (US 6,379,745 B1).

Referring to column 17, line 55 to column 19, line 55, Kydd et al. disclose a method of forming conductor images that includes adding a photo patterned polyimide layer to an IC chip surface, filling the patterned polyimide layer by doctor blading a conductive ink, and curing the conductive ink to form conductive traces. The conductive ink includes copper as indicated in column 19, line 65 to column 20, line 24.

These are all of the process limitations as set forth in claims 1-6, 14, 16-17 of the applicant's invention as well as all of the structural limitations as set forth in claims 11-12 of the applicant's invention.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stepan in view of Capote et al. (US 5,716,663).

Referring to Figs. 1-2 and column 2, lines 7-50, Stepan discloses a method of forming a conductive pattern that includes depositing an insulating coating (10) on a substrate (16), forming channels (13) in the insulating coating (10) by stamping, and filling the channels (13) with conductive paste. These are limitations as set forth in claims 14-16 of the applicant's invention.

However, Stepan does not expressly teach or suggest blading the conductive paste into the channels, which is a limitation of independent claim 14.

Capote et al. teach that grooves formed in an insulator can be filled with conductive ink by doctor blading (see column 12, lines 14-21).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Stepan and Capote et al. in order to apply the conductive paste of Stepan by doctor blading, as taught by Capote et al., because Capote et al. show that doctor blading is a known way in the art for filling grooves with conductive material.

9. Claims 3, 5-8, 14, 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over De Bruin et al. (US 5,063,169) as applied to claims 1-2, 4 above, and further in view of Capote et al. (US 5,716,663).

As shown above, De Bruin et al. anticipate claims 1-2, 4 of the applicant's invention. These are also limitations as set forth in claims 14, 16-17 of the applicant's invention. Further, De Bruin et al. disclose the subsequent removal of the resist layer (13) by etching as described in column 5, lines 25-44 (the limitation of claim 7) and depositing an aluminum layer (21) over the conductive pillars (15) as described in column 5, line 66 to column 6, line 7 (the limitation of claim 8).

However, De Bruin et al. do not expressly teach or suggest using a blading technique (limitations of claims 3, 14), using a conductive ink (the limitation of claim 5), nor curing the material (the limitation of claim 6).

Referring to Fig. 7 and column 11, line 58 to column 12, line 33, Capote et al. teach a method for producing multilayer circuits that includes filling grooves formed in a dielectric layer with conductive ink by doctor blading and subsequently curing the conductive ink.

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the teachings of De Bruin et al. by substituting the doctor blading method of Capote et al. for the plating method of De Bruin et al. because Capote et al. show that doctor blading a conductive ink combined with curing is another way to form embedded conductive structures in insulators.

10. Claims 9-10, 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Capote et al. (US 5,716,663) as applied to claims 1, 11 above, and further in view of Kodas et al. (US 2003/0108664 A1).

As shown above, Capote et al. anticipate claims 1, 11 of the applicant's invention. However, Capote et al. do not expressly teach or suggest that their conductive circuits can be used as conductors in active matrix liquid crystal displays, which are the further limitations to claim 1 as set forth in 9-10 of the applicant's invention and the further limitation to claim 11 as set forth in claim 13 of the applicant's invention. Kodas et al. teach that precursor compositions corresponding to electrical conductors formed in recessed features of an insulating substrate can be used as interconnects for active matrix liquid crystal displays (see abstract and paragraphs [0362] to [0364]).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Capote et al. and Kodas et al. in order to use the conductive circuits of Capote et al. as interconnects for active matrix

liquid crystal displays, as taught by Kodas et al., because Kodas et al. recognize that the interconnects can advantageously be formed by inexpensive methods.

11. Claims 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stepan and Capote et al. (US 5,716,663) as applied to claim 14 above, and further in view of Kodas et al. (US 2003/0108664 A1).

As shown above, the combination of Stepan and Capote et al. has all of the limitations as set forth in claim 14 of the applicant's invention. These are also limitations as set forth in independent claim 19 of the applicant's invention. However, this combination does not expressly teach or suggest that the conductive circuits can be used as conductors in active matrix liquid crystal displays, which are the further limitation to claim 14 as set forth in 18 of the applicant's invention and a limitation as set forth in claim 19 of the applicant's invention. Kodas et al. teach that precursor compositions corresponding to electrical conductors formed in recessed features of an insulating substrate can be used as interconnects for active matrix liquid crystal displays (see abstract and paragraphs [0362] to [0364]).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Stepan, Capote et al., and Kodas et al. in order to use the conductive circuits of Stepan and Capote et al. as interconnects for active matrix liquid crystal displays, as taught by Kodas et al., because Kodas et al. recognize that the interconnects can advantageously be formed by inexpensive methods.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen W. Smoot whose telephone number is 571-272-1698. The examiner can normally be reached on Monday to Friday from 8:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra V. Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Stephen W Smoot/
Primary Examiner
Art Unit 2813

sws